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## FOREIGN PATENT DOCUMENTS

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## **NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	υ	S.S. Chung et al., "A Novel and Direct Determination of the Interface Traps in Sub-100nm CMOS Devices with Direct Tunnelin Regime (12~16A) Gate Oxide," 2002 Symposium On VLSI Technology Digest of Technical Papers, pages 74-75.				
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